[Claim(s)]

[Claim 1] The history of the request address from a processor to cache memory and difference with the address of the past are held. When a difference with the history of the address concerning the present request and said request address is equal to said address difference The prefetch control unit characterized by directing prefetch to said cache memory by the address which added said address difference to the address concerning the new request concerned.

[Claim 2] The address history table holding the history of the request address from a processor to cache memory, and difference with the address of the past, The subtractor which reduces and outputs the address concerning the present request from the history of said request address held at this address history table, The adder which adds and outputs the output of this subtractor, and the address concerning said present request, The prefetch control unit characterized by including the address control circuit which publishes a prefetch request by making the output of said adder into a prefetch address when the output of said subtractor is equal to said difference held at said history table.

[Claim 3] The coincidence comparison machine which detects whether said address control circuit has the output of said subtractor equal to said difference held at said history table is included. The prefetch control unit according to claim 2 characterized by publishing a prefetch request by making the output of said adder into a prefetch address when the purport that this coincidence comparison machine is equal is detected.

[Claim 4] Said address control circuit contains the address range register to which a range

value permissible as said difference of said address history table is set. The prefetch control unit according to claim 2 characterized by making the output of said subtractor hold to said difference of said history table if the output of said subtractor is in the range value set as said address range register.

[Claim 5] Said address control circuit contains the range comparator which the output of said subtractor is in the range value set as said address range register, or detects no. The prefetch control unit according to claim 4 characterized by making the output of said subtractor hold to said difference of said history table when it detects that this range comparator is within the limits.

[Claim 6] [ said address control circuit ] The prefetch control unit according to claim 5 characterized by setting said difference as the value of said address range register out of range while registering the address concerning said present request into said history of said history table, when it detects that said range comparator is out of range.

[Claim 7] The address history table holding at least 2 sets of groups which consist of a history of the request address from a processor to cache memory, and difference with the address of the past, Two or more subtractors which reduce the address concerning the present request, respectively and output it from each of the history of said request address held at this address history table, The adder which chooses any of the output of the subtractor of these plurality they are, and adds and outputs the selector to output, and the output chosen by this selector and the address concerning said present request, When said corresponding difference and corresponding equal which are the output of two or more of said subtractors, and were held at said history table exist, while controlling said selector to choose the output of the subtractor concerned The prefetch control unit characterized

by including the address control circuit which publishes a prefetch request by making the output of said adder into a prefetch address.

[Claim 8] Two or more coincidence comparison machines which detect whether each output of two or more of said subtractors of said address control circuit is equal to said corresponding difference held at said history table are included. The prefetch control unit according to claim 7 characterized by publishing a prefetch request by making the output of said adder into a prefetch address when a purport with any of these coincidence comparison machine equal they are is detected.

[Claim 9] Said address control circuit contains the address range register to which a range value permissible as said difference of said address history table is set. The prefetch control unit according to claim 7 characterized by making the output of said subtractor hold to said difference to which said history table corresponds if which output of two or more of said subtractors is in the range value set as said address range register.

[Claim 10] Said address control circuit contains two or more range comparators which each output of two or more of said subtractors is in the range value set as said address range register, or detect no. The prefetch control unit according to claim 9 characterized by making the output of said subtractor hold to said difference [ / table / said / history ] when it detects that either of these ranges comparators is within the limits.

[Claim 11] [ said address control circuit ] When it detects that said range comparator is out of range, while registering the address concerning said present request into said which history of said history table The prefetch control unit according to claim 10 characterized by setting said corresponding difference as the value of said address range register out of range.

[Claim 12] The cache memory connected between a processor, a primary storage, and said processor and said primary storage, In the information process system containing the prefetch control unit which publishes a prefetch request from said processor to said cache memory based on the request address to said cache memory The address history table on which said prefetch control unit holds the history of the request address from said processor to said cache memory, and difference with the address of the past, The subtractor which reduces and outputs the address concerning the present request from the history of said request address held at this address history table, The adder which adds and outputs the output of this subtractor, and the address concerning said present request, The information process system characterized by including the address control circuit which publishes a prefetch request by making the output of said adder into a prefetch address when the output of said subtractor is equal to said difference held at said history table.

[Claim 13] The queue with which said cache memory holds a waiting request, The information process system according to claim 12 characterized by including the canceller which cancels the prefetch request from said prefetch control unit when the request which exceeds a predetermined number at this queue is held.

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the prefetch control unit which detects the regularity of an address and performs prefetch operation about a prefetch

control unit.

[0002]

[Description of the Prior Art] Conventionally, when the phenomenon (henceforth a cache miss) in which required data does not exist in cache memory occurred, it was controlling by this kind of cache memory control unit to transmit required data from a storage apparatus to cache memory. For example, in the JP,59-96585,A gazette, the cache memory control unit which gives a data demand to the both sides of cache memory and a storage apparatus at the time of a cache miss is indicated.

[0003] Moreover, as a method which controls cache memory from software, the data which is probably needed in the future was specified by the software instruction, and it was controlling to transmit required data from a storage apparatus to cache memory beforehand. For example, "1992 year 2 Moon, IEEE comp contest 92 collected papers (C. Dowdell and L.Thayer) : [ "Scalable Graphics Enhancements for PA-RISC Workstations", Proc.of IEEE COMPCON 92, pp.122-128, and Feb.1992." ] The cache prefetch command (fetch32) it is directed that carries out block transfer of 32 bytes of data to a data cache is indicated.

[0004]

[Problem to be solved by the invention] However, in order to start access to a storage apparatus ignited by a cache miss, to the former conventional cache memory control unit, time was taken for a central processing unit to receive data, and there was a problem that the command which needs the data could not be continued, with it. Moreover, although the central processing unit in recent years aimed at the improvement in throughput performance by adopting pipeline composition, for the cache miss, the whole pipeline is

stopped and this had become evil for the improvement in effective performance of a central processing unit.

[0005] Moreover, by the method of depending on the latter conventional cache prefetch command, in order to have to direct prefetch operation clearly on a program by this prefetch command, program quantity increases, command supply is checked and it results in having a bad influence on effective performance. Furthermore, since it was generally impossible, it was difficult to generate a prefetch command in the suitable position on a program to compile time to grasp completely the address which accesses a storage apparatus before program execution.

[0006] When a processor accesses the purpose of this invention in order by fixed address difference, it predicts the access and there is in offering the prefetch control unit which raises system performance by prefetching to cache memory in advance.

[0007]

[Means for solving problem] In order to solve the above-mentioned technical problem [ the prefetch control unit of this invention ] The history of the request address from a processor to cache memory and difference with the address of the past are held. When a difference with the history of the address concerning the present request and said request address is equal to said address difference, prefetch is directed to said cache memory by the address which added said address difference to the address concerning the new request concerned.

[0008] [ moreover, other prefetch control units of this invention ] The address history table holding the history of the request address from a processor to cache memory, and difference with the address of the past, The subtractor which reduces and outputs the

address concerning the present request from the history of said request address held at this address history table, The adder which adds and outputs the output of this subtractor, and the address concerning said present request, When the output of said subtractor is equal to said difference held at said history table, the address control circuit which publishes a prefetch request by making the output of said adder into a prefetch address is included.

[0009] Moreover, in other prefetch control units of this invention [ said address control circuit ] Including the coincidence comparison machine which detects whether the output of said subtractor is equal to said difference held at said history table, when the purport that this coincidence comparison machine is equal is detected, a prefetch request is published by making the output of said adder into a prefetch address.

[0010] Moreover, in other prefetch control units of this invention [ said address control circuit ] If it is in the range value with which the output of said subtractor was set as said address range register, the output of said subtractor will be made to hold to said difference of said history table including the address range register to which a range value permissible as said difference of said address history table is set.

[0011] Moreover, in other prefetch control units of this invention [ said address control circuit ] When it detects that this range comparator is within the limits including the range comparator which is in the range value with which the output of said subtractor was set as said address range register, or detects no, the output of said subtractor is made to hold to said difference of said history table.

[0012] Moreover, in other prefetch control units of this invention [ said address control circuit ] When it detects that said range comparator is out of range, while registering the

address concerning said present request into said history of said history table, said difference is set as the value of said address range register out of range.

[0013] [ moreover, other prefetch control units of this invention ] The address history table holding at least 2 sets of groups which consist of a history of the request address from a processor to cache memory, and difference with the address of the past, Two or more subtractors which reduce the address concerning the present request, respectively and output it from each of the history of said request address held at this address history table, The adder which chooses any of the output of the subtractor of these plurality they are, and adds and outputs the selector to output, and the output chosen by this selector and the address concerning said present request, When said corresponding difference and corresponding equal which are the output of two or more of said subtractors, and were held at said history table exist, while controlling said selector to choose the output of the subtractor concerned The address control circuit which publishes a prefetch request by making the output of said adder into a prefetch address is included.

[0014] Moreover, in other prefetch control units of this invention [ said address control circuit ] Two or more coincidence comparison machines which detect whether each output of two or more of said subtractors is equal to said corresponding difference held at said history table are included. When a purport with any of these coincidence comparison machine equal they are is detected, a prefetch request is published by making the output of said adder into a prefetch address.

[0015] Moreover, in other prefetch control units of this invention [ said address control circuit ] The address range register to which a range value permissible as said difference of said address history table is set is included. If which output of two or more of said

subtractors is in the range value set as said address range register, the output of said subtractor will be made to hold to said difference to which said history table corresponds.

[0016] Moreover, in other prefetch control units of this invention [ said address control circuit ] When it detects that either of these ranges comparators is within the limits including two or more range comparators which are in the range value with which each output of two or more of said subtractors was set as said address range register, or detect no, the output of said subtractor is made to hold to said difference [ / table / said / history ].

[0017] Moreover, in other prefetch control units of this invention [ said address control circuit ] Said difference which corresponds while registering the address concerning said present request into said which history of said history table, when it detects that said range comparator is out of range is set as the value of said address range register out of range.

[0018] Moreover, the cache memory to which the information process system of this invention is connected between a processor, a primary storage, and said processor and said primary storage, The prefetch control unit which publishes a prefetch request from said processor to said cache memory based on the request address to said cache memory is included. The address history table on which said prefetch control unit holds the history of the request address from said processor to said cache memory, and difference with the address of the past, The subtractor which reduces and outputs the address concerning the present request from the history of said request address held at this address history table, The adder which adds and outputs the output of this subtractor, and the address concerning said present request, When the output of said subtractor is equal

to said difference held at said history table, the address control circuit which publishes a prefetch request by making the output of said adder into a prefetch address is included.

[0019] Moreover, in other information process systems of this invention [ said cache memory ] The queue holding a waiting request and the canceller which cancels the prefetch request from said prefetch control unit when the request which exceeds a predetermined number at this queue is held are included.

[0020]

[Mode for carrying out the invention] Next, the form of operation of the prefetch control unit of this invention is explained in detail with reference to Drawings.

[0021] Reference of drawing 1 will apply the form of operation of the prefetch control unit of this invention to the information process system containing a processor 100, cache memory 300, and a primary storage 400. The prefetch control unit 200 is connected between a processor 100 and cache memory 300. Cache memory 300 and a primary storage 400 are connected by the system bus 500.

[0022] If a processor 100 publishes an access request with a signal line 101, if cache memory 300 has data concerning the request concerned (cache hit), it will send the data to a processor with a signal line 301. If cache memory 300 does not have data concerning the request concerned (cache miss), cache memory 300 accesses a primary storage 400 through a system bus 500, and reads corresponding data. The read data is sent to a processor 100 with a signal line 301 while it is held at cache memory 300.

[0023] The prefetch control unit 200 supervises the access request 101 from a processor 100, and if the access request accessed in order by fixed address difference is detected, it will publish a prefetch request to cache memory 300. If the prefetch control unit 200

publishes a prefetch request with a signal line 201, if cache memory 300 is a cache hit, it will not carry out special operation, but if it is a cache miss, will access a primary storage 400 through a system bus 500, and will read corresponding data. Although the read data is held at cache memory 300, it is not sent to a processor 100.

[0024] Cache memory 300 is made to process by giving priority to the access request from a processor 100 over the prefetch request from the prefetch control unit 200.

[0025] In addition, about a processor 100, cache memory 300, and a primary storage 400, unless it mentions specially, the same thing as the usual technology is used.

[0026] When drawing 2 is referred to, [ the prefetch control unit 200 ] The request address register 210 holding the address concerning an access request, The address history table 220 holding the history of the accessed address, The subtractor 240 which generates the address difference between the adder 230 which generates a prefetch address, and the address currently held at the address history table 220 and the address currently held at the request address register 210, The selector 280 which chooses one output of the subtractors 240, and the address control circuit 290 which publishes a prefetch request to cache memory 300 while updating the address history table 220 according to the address difference by subtractor 240 are included.

[0027] Among the access requests by a signal line 101, the portion of an address is held at the request address register 210 until a series of following processings are completed. The address history table 220 makes a group "difference" with the address before accessing the "history address" which is an address accessed in the past, and its address, and is held. Subtractor 240 subtracts the address held at the address history table 220 from the address held at the request address 210, and generates "address difference." A

selector 280 chooses the address difference from subtractor 240 with directions of the address control circuit 290. An adder 230 generates the address which should add the address held at the request address register 210, and the address difference chosen by the selector 280, and should become in a prefetch address.

[0028] If drawing 3 is referred to, in the more detailed block diagram of the prefetch control unit 200, the history address 221 and difference 222 constitute the address history table 220 in drawing 2 . Moreover, the address range register 260, a comparator 291, a comparator 292, and the table control circuit 293 constitute the address control circuit 290 in drawing 2 . With the form of operation of drawing 3 , although four are made into the example for the number of history addresses, in this invention, the number of history addresses can choose one or more arbitrary numbers.

[0029] A comparator 291 compares the output and difference 222 of the subtractor 240 which corresponds, respectively, and outputs whether it is in agreement. This comparator 291 also calls it a coincidence comparison machine. A range value permissible as address difference which the address range register 260 should detect is set up. That is, the value of the range permissible as a value registered as difference 222 is set up. A comparator 292 outputs whether the output of subtractor 240 is included within limits set as the address range 260. This comparator 292 also calls it a range comparator. The table control circuit 293 gives a control signal to a selector 280 by the below-mentioned operation, and ** updates the address history table 220. Moreover, the table control circuit 293 controls whether a prefetch request is published about the address from an adder 230 by the below-mentioned standard.

[0030] Reference of drawing 4 will generate the address which should turn into a prefetch

address as follows with the form of operation of this invention. Supposing the address (for example, "$5000") which accessed the history address 221 last time beforehand is held Subtractor 240 subtracts the address held at the history address 221 from the address (for example, "$5100") held at the request address register 210, and generates address difference (here "$0100"). Supposing this address difference is chosen by the selector 280, an adder 230 will generate an address (here "$5200") by adding the address held to this address difference at the request address register 210.

[0031] Next, operation in the form of operation of the prefetch control circuit of this invention is explained.

[0032] Reference of drawing 3 and drawing 5 will set first a range value permissible as address difference which should be detected to the address range register 260 (Step S901).

[0033] If a new address is held at the request address register 210, each of subtractor 240 will subtract the address held at the request address register 210 from the address held at the corresponding history 221 (Step S902).

[0034] Coincidence with the difference 222 which corresponds about the subtraction result (address difference) of subtractor 240 is detected by the comparator 291 (Step S903). If there is a match, the congruous address differences will be chosen by the selector 280. Arbitrary one is chosen when two or more coincidence is detected. This selected address difference is inputted into an adder 230, and a prefetch address is generated. The table control circuit 293 publishes a prefetch request through a signal line 201 by this prefetch address (Step S904). The table control circuit 293 makes the address currently held at the request address 210 hold to the group chosen by the selector 280 of

the address history tables 220, after publishing a prefetch request (Step S905).

[0035] Moreover, in Step S903, when a match is not detected, it is judged by the comparator 292 whether each of the address difference by subtractor 240 is contained in the address range set as the address range register 260 (Step S906). Since it means that access of fixed address difference did not continue in order when it is judged that it is contained in an address range in this step S906, a prefetch request does not publish. In this case, if contained in the address range, while choosing the address difference of the group which the comparator 292 detected by a selector 280 and updating the history address 221 of that group with the request address register 210 The difference 222 of the group is updated by the address difference chosen by the selector 280 (Step S907).

[0036] Since it means being single shot access and access to the new field which is not in the history by the present when it is judged that it is outside an address range in Step S906, a prefetch request does not publish. In this case, the table control circuit 293 carries out the zero clear of the corresponding difference 222 while newly registering the value of the request address register 210 using a certain group in the address history table 220 (Step S908). You may make it whether which group is used here use the group from which arbitrary groups are sufficient and coincidence by a comparator 291 is not detected most for many years. The zero clear of the difference 222 needed to be carried out because it was not carried out within the limits at Step S906 next time, and it does not need to be zero, and should just be the value out of range set as the address range register 260.

[0037] After Step S905, S907, or processing of S908 returns to processing of Step S902 again, and if an address is held next at the request address register 210, it will calculate

address difference.

[0038] Next, the example of processing by the form of operation of this invention is explained.

[0039] If drawing 6 (a) is referred to, it will be considered as "5000" and the thing by which "900" and the address range 260"20-500" are held at difference 222 as an initial state at the history address 221. If "3000" is held in this state at the request address register 210, in the output of a comparator 291, the output of an "inequality" and a comparator 292 will become "out of range." Therefore, while the address of the request address 210 is registered into the history address 221 in this case, the zero clear of the difference 222 is carried out (Step S908 of drawing 5 ).

[0040] If drawing 6 (b) is referred to and "3100" will be held next at the request address register 210, as for the output of a comparator 291, the output of an "inequality" and a comparator 292 will become "within the limits." Therefore, while the history address 221 is updated by address"3100" of the request address 210 in this case, address difference"100" is set to difference 222 (Step S907 of drawing 5 ).

[0041] If drawing 6 (c) is referred to and "3200" will be held next at the request address register 210, as for the output of a comparator 291, "coincidence" and the output of a comparator 292 will become "within the limits." Therefore, while a prefetch request is published by address"3300" which an adder 210 outputs in this case, the history address 221 is updated by address"3200" of the request address 210 (Steps S904 and S905 of drawing 5 ). Thereby, as long as the request address increases by constant value "100" every, it can precede with it and a prefetch request can be published henceforth.

[0042] In addition, a write-through can also be carried out although the form of above-

mentioned operation explained cache memory 300 as what takes a copy back method. In that case, what is necessary is to process only the read access from a processor 100 as an access request in the prefetch control unit 200, in order that there may be no meaning in prefetching to the right access from a processor 100.

[0043] Thus, with the form of above-mentioned operation, the difference of the address held at the target history 221 and the address held at the request address register 210 is calculated, and as long as the address difference is in agreement with difference 222, a prefetch request can be published. Moreover, since the value of difference 222 will be reset up if there is a continuous address within limits installed in the address range register 260 even when the value of difference 222 has disappeared, subsequent prefetch requests are attained.

[0044] Next, the form of other operations of this invention is explained.

[0045] Although the fundamental composition of the form of other operations of this invention is the same as that of the form of above-mentioned operation, cache memory 300 is improved.

[0046] [ the cache memory 300 in the form of other operations ] if drawing 7 is referred to The waiting queue 321 for an input which manages the waiting request for access to the cache core 320, The waiting queue 331 for an output which manages the waiting request for access from the cache memory core 320 to the bus access control circuit 330, The canceller 310 which supervises the waiting state in the waiting queue 321 for these inputs and the waiting queue 331 for an output with signal lines 322 and 332, and performs cancellation processing of a prefetch request is included. Here, the cache memory core 320 points out the main part for functioning as cache memory, such as an

address array and a data array. Moreover, the bus access control circuit 330 performs control for sending out the data outputted from the cache memory core 320 to a system bus 500.

[0047] The number register 312 of the waiting for an input which will hold the number [ in / in a canceller 310 / the waiting queue 321 for an input ] of waiting requests if drawing 8 is referred to, The number register 313 of the waiting for an output holding the number of waiting requests in the waiting queue 331 for an output, The number upper-limit register 314 of the waiting for an input holding a upper limit permissible as the number of the waiting requests for an input and the number upper-limit register 315 of the waiting for an output holding a upper limit permissible as the number of the waiting requests for an output are included. Moreover, the comparator 316 which detects that a canceller 310 has the value of the number register 312 of the waiting for an input larger than the value of the number upper-limit register 314 of the waiting for an input, The comparator 317 which detects that the value of the number register 313 of the waiting for an output is larger than the value of the number upper-limit register 315 of the waiting for an output, OR circuit 318 which generates a prefetch halt control signal when any of comparators 316 and 317 they are outputs a detection signal, and the switch 319 which controls whether it lets the prefetch request 201 pass according to a prefetch halt control signal are included.

[0048] A suitable upper limit shall be beforehand set to the number upper-limit register 314 of the waiting for an input, and the number upper-limit register 315 of the waiting for an output. If the number of waiting requests in the waiting queue 321 for an input exceeds the value of the number upper-limit register 314 of the waiting for an input or the

number of waiting requests in the waiting queue 331 for an output exceeds the value of the number upper-limit register 315 of the waiting for an output The output of OR circuit 318 is asserted and a switch 319 is changed into an open state. Thereby, the prefetch request 201 is no longer sent to the cache memory core 320.

[0049] Thus, since the prefetch request 201 is canceled with the form of other above-mentioned operations when the load of cache memory 300 or a system bus 500 is high, Prefetch of the low data of a possibility of being used can be deterred and the system performance as the whole can be raised.

[0050]

[Effect of the Invention] As opposed to access of the fixed address gap which a processor accesses by the above explanation according to this invention so that clearly Next, the address accessed is predicted, since data can be prefetched and set from a main memory to cache memory in advance, the substantial access time of a processor can be shortened and system performance can be raised. Since unnecessary prefetch is not performed on the other hand when not accessed at intervals of a fixed address, the cache memory of small capacity can be utilized effectively and system performance can be raised.